Docket No.: 071971-0566

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 53080

Tsuyoshi MATSUSHITA

Confirmation Number: Not Yet Assigned

Application No.: 10/575,098

Group Art Unit: Not Yet Assigned

Filed: April 10, 2006

Examiner: Not Yet Assigned

For: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING THE

SAME

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The Customer Number for the above listed application should be:

53080

It is requested that the U.S. Patent and Trademark Office records be updated to reflect this correction. Thank you.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

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Date: September 13, 2007



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Applicant:	Tsuyoshi MATSUSHITA Docket	I No	971-0566	Serial No.	Not Yet Assigned		
Title:	LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING THE SAME Patent No.						
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Docket No.: 071971-0566

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In re Application of : Customer Number: 53080

Tsuyoshi MATSUSHITA : Confirmation Number: Not Yet Assigned

Application No.: 10/575,098 : Group Art Unit: Not Yet Assigned

Filed: April 10, 2006 : Examiner: Not Yet Assigned

For: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING THE

SAME

LETTER TO SUBMIT FRONT PAGE OF INTERNATIONAL PUBLICATION AND ENGLISH-TRANSLATED INTERNATIONAL SEARCH REPORT

Mail Stop OIPE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Attached are copies of the front page of the International Publication and the English translation of the International Search Report received from the International Bureau of WIPO for the corresponding PCT application of the above-referenced application. It is requested that the U.S. Patent and Trademark Office records be updated to include these documents. Thank you.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogart

Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W. Washington, DC 20005-3096 Phone: 202.756.8000 MEF:ln

Facsimile: 202.756.8087

Date: September 13, 2007

P. 02/04

(12) 特許協力条約に基づいて公開された国際出願

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- (21) 国際出願番号:

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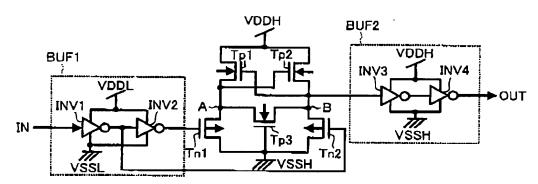
神順2005-041291 2005年2月17日(17.02,2005)

- (71) 出願人(米国を除く全ての指定国について): 松下電 器產業株式会社(MATSUSHITA ELECTRIC INDUS-TRIAL CO., LTD.) [JP/JP]; 〒5718501 大阪府門真市大 字門真1006番地 Osaka (JP).
- (72) 発明者; および
- (75) 発明者/出願人 (米国についてのみ): 松下 剛 (MAT-SUSHITA, Tsuyoshi).

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- (81) 指定国(表示のない限り、全ての種類の国内保護が 可能); AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
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- (54) Title: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT HAVING THE SAME
- (54) 発明の名称: レベルシフト回路及びこれを備えた半導体集積回路



(57) Abstract: A level shift circuit comprising two N-ch transistors (Tn1, Tn2) that receive a pair of complementary input signals; and two P-ch transistors (Tp1,Tp2) that have their gate terminals cross-coupled to each other; wherein nodes (A.B), which are the drains of the two N-ch transistors (In1,Tn2) and which operate inversely to each other, are connected to each other at a resistor (Tp3). The resistor (Tp3), which comprises a P-ch transistor, has its gate grounded and is always conductive. For example, when the N-ch transistor (Tn1) is turned on and the N-ch transistor (Tn2) is turned off, a current initially flows from the node (A) exhibiting a higher potential through the resistor (Tp3) to the node (B) exhibiting a lower potential, which results in a rise of the potential at the node (B). Therefore, the potential rise at the node (B) is promoted as compared with a case where only the P-ch transistor (Tp2) is turned on. Thus, the level shift circuit having a less number of elements can operate in a higher rate,

(57) 要約: レベルシフト回路において、一対の相補入力信号を受ける2つのNchトランジスタTn1、Tn2と、 ゲート端子が互いにクロスカップル接続された2つのPchトランジスタTp1、Tp2とを備えたレベルシフト 回路において、前記2つのNchトランジスタTn1、Tn2のドレインであって互いに反転動作しているノード A、日同士が、抵抗Tp3で接続される。この抵抗Tp3は、Pchトランジスタで構成され、そのゲートは接地 🔁 されて、常時導通状態にある。例えば、NchトランジスタTn1がONL、Tn2がOFFする際には、その当 初で、高電位側のノードAから電流が抵抗Tp3を通じて低電位側のノード日に流れて、低電位側のノード日の電 位が上昇する。従って、このノード日の電位上昇は、PchトランジスタTp2のONのみによる場合に比べて促 進される。従って、レベルシフト回路を少ない素子数でもって高速動作できる。

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R:606

OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:

一 国際調査報告書

2文字コード及び他の略語については、定期発行される 各PCTガゼットの巻頭に掲載されている「コードと略語 のガイダンスノート」を参照。

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	INTERNATIONAL SEARCH REPORT		nsl application No.
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Kokai J	Jitsuyo Shinan Koho 1971-2006 To	itsuyo Shinan Toroku K oroku Jitsuyo Shinan K	aho 1996-2006 aho 1994-2006
	base consulted during the international search (name of	f data base and, where practicable,	search terms used)
	NTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where ap		
•	JP 2001-298356 A (Matsushita Industrial Co., Ltd.), 26 October, 2001 (26.10.01), Par. Nos. [0066] to [0091]; & US 2001/0013795 A1 & EP & EP 1263142 A1	Figs. 7 to 18	1-8
A	JP 2003-152096 A (Hitachi, I 23 May, 2003 (23.05.03), Par. No. [0052], example 4 to Fig. 12 & US 2003/0042965 Al & US & CN 1407724 A	o Par. No. [0055];	1-8
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